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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/749,464	12/31/2003	Derek A. Thompson	INTEL4	3974

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EXAMINER	
THOMAS, SHANE M	
ART UNIT	**PAPER NUMBER**
2186	

DATE MAILED: 05/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/749,464	THOMPSON ET AL.	
	Examiner	Art Unit	
	Shane M. Thomas	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office action is responsive to the application filed 12/31/03. Claims 1-15 are presented for examination and are currently pending.

In the response to this Office action, the Examiner politely requests that support be shown for language added to any original claims on amendment and any new claims. That is, indicate support for newly added claim language by specifically pointing to page(s) and line numbers in the specification and/or drawing figure(s). This will assist the Examiner in prosecuting this application.

Excerpts from all prior art references cited in this Office action shall use the shorthand notation of [column # / lines A-B] to denote the location of a specific citation. For example, a citation present on column 2, lines 1-6, of a reference shall herein be denoted as "[2/1-6]."

Specification

The disclosure is objected to because of the following informalities:

(i) the word --is-- should be corrected to --are-- (¶1, third line from bottom);

(ii) the term --vectors-- should be corrected to --vector-- (¶8 - page 4, line 1);

(iii) the word "beconnected" should be corrected to "be connected" (¶13, line 2);

Appropriate correction is required.

The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any remaining errors of which Applicant may become aware in the specification.

Claim Objections

Claims 2-4 and 6-10 are objected to because of the following informalities:

As per claim 2, the acronym "CS" should be spelled out for the instance the term is used in the claims. The Examiner recommends amending the term "CS" to "chip select (CS)."

As per claim 4, the term "claim1" should be corrected to "claim 1."

As per claim 6, lines 7-8 of the claim read awkwardly; the Examiner recommends removing the word "based" as the word does not seem to be appropriate in the claim language.

As per claim 9, line 4 appears either incomplete or comprises a typographical error. The word "using" should be removed.

Claims 3,7,8,10, are objected to as being dependent upon objected to base claims.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1-15 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

As per claim 1-15, the Applicant makes reference to a logical chip select "vector" but does not specifically detail in the specification what exactly this "vector" comprises. For

example, ¶6 of the specification as originally filed, states "Thus, the logical chip select vectors may be used to fill the DIMM memory modules in a sequential manner ..." This instance is the first in which Applicant discusses the term "vector" in the specification. It is not clear to the Examiner if Applicant is referring to the collection of all chip select bits (i.e. CS(0) : CS(7) equals a "logical chip select vector, where "different " chip select vectors are generated by different combinations of the setting to active/inactive of the individual CS(x) bits), a subset of the chip select signals that correspond to a given DIMM module (i.e. such as CS(0) : CS(1) comprise a CS vector as they both correspond to DIMM#0 in the example of ¶7 of Applicant's specification), or if another definition was intended as the terms "logical chip select vector" and "physical chip select vector" are not described in the specification to enable one skilled in the art to make and/or use the present invention of the Applicant.

Nonetheless, for the purposes of examination, the Examiner has considered a logical chip select vector to be a collection of bits that relate to the determination of chip select signals. No new matter may be presented.

As per claim 6, the Examiner fails to see how a "physical chip select vector" can be "physically connected" to at least one of the plurality of memory modules, as the "physical chip select vector" appears to simply be data, per se, (refer to Applicant's figure 2) and not comprise a physical medium whatsoever. Therefore, the limitations of claim 6 are not enabled as they are not described in the specification to enable one skilled in the art to make and/or use the present invention of the Applicant.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-5 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claim 1, throughout the Applicant's specification, no mention is made of receiving *an address* of a logical chip select vector (just the logical chip select vector itself - ¶8). Nonetheless, for the purposes of examination, the Examiner has considered the phase "receiving an address of a logical chip select vector" as "receiving an address comprising a logical chip select vector."

Claims 2-5 are rejected as being dependent upon a rejected base claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1,5,6,7, and 14 are rejected under 35 U.S.C. 102(e) as being anticipated by Sandorfi (U.S. Patent No. 6,836,818).

As per claim 1, Sandorfi teaches in [10/15 - 11/18] **receiving an address of a logical chip select vector** (0820 1234h, which is a collection of bits [in hexadecimal format] that relate to chip selects, as discussed herein and in the passage of Sandorfi) **for at least one memory module 48** [5/28-35] **converting the logical chip select vector to a corresponding physical chip select vector associated with a physical location of the at least one memory module that is different than the logical chip select vector** [10/32-41 and 11/3-11], and **accessing the memory module using the physical chip select vector** (07FC 1234h) [11/15-18].

As per claim 5, Sandorfi teaches **wherein the memory module** 48 **is a DRAM** [5/28-35].

As per claim 6, Sandorfi teaches **a memory controller** 64 (figure 3) **operable to generate a logical chip select vector** (0820 1234h) **based on a one-to-one relationship between a memory map and a plurality of memory modules** 48 (it can be seen that Sandorfi's system is mapped in a one-to-one relationship as each physical memory address maps to one and

only one physical memory address - refer to the mapping shown in figure 3D to verify the one-to-one correspondence) [10/15-11/18], **at least one physical chip select vector** (07FC 1234h - [10/35-41]) **connected to at least one of the plurality of memory modules** (can be seen since the physical chip select allows for accessing the respective physical address of the memory 48 - [10/15-31]), **a chip select remapping unit** (shown in figure 3D) **operable to convert a logical chip select vector to a physical chip select vector** (shown in 3D and discussed in [10/32-11/18], **and wherin the physical chip select vector is operable to allow the memory controller** 64 **to access memory modules** [11/15-18] (i.e. once converted, the physical chip select vector is where the memory 48 is accessed, not the logical chip select vector).

As per claim 7, Sandorfi teaches **a central processing unit** 46 (figure 3) **operable to instruct the memory controller** 64 **to access at least one of the memory modules** (via control signals, as shown - [7/53-8/29].

As per claim 14, Sandorfi teaches **a plurality of chip select vectors** (bits 0820 1234h as shown in figure 3D) **based on a one-to-one relationship between a memory map and a plurality of memory modules** 48 (it can be seen that Sandorfi's system is mapped in a one-to-one relationship as each physical memory address maps to one and only one physical memory address - refer to the mapping shown in figure 3D to verify the one-to-one correspondence) [10/15-11/18], **a plurality of logical AND components** 202 (figure 3D) **having a plurality of inputs and a single output, wherein at least one input of each logical AND component is one of the logical chip select vectors** (shown), **a control vector** 200 **comprising a plurality of bits, wherein at least one bit is connected to an input of each logic AND component, and is operable to control the output of each logical AND component** (as shown). Further in figure

3d, Sandorfi teaches **a plurality of OR components** 209, **wherein each logical OR component comprises a plurality of inputs and single output, wherein the inputs of the logical OR component are the outputs of each of the logical AND components** (shown) **and the output of each logical OR component represents at least one physical chip select vector** (final chip select 07FC 1234h as discussed in [10/32-11/18]).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 4,9,10, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sandorfi (U.S. Patent No. 6,836,818) in view of Haas et al. (U.S. Patent Application Publication No. 2004/0215906).

As per claims 4, 10, and 15, Sandorfi does not specifically teach **wherein the memory module is a DIMM**, however Sandorfi does teach [5/28-35] that the memory 48 may comprise two 64 MB banks of SDRAM (or RDRAM). Haas teaches (¶6) a system that comprises two banks of DIMM for memory mirroring purposes. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have combined the system of Sandorfi with the teaching of dual DIMM module banks of Haas in order to have (1) gained

the benefit of increased RAM storage ([5/28-35] of Sandorfi) and (2) gained the ability to mirror data to another DIMM RAM module to maintain data integrity (¶6, Hass).

As per claim 9, Sandorfi does not specifically teach mapping the logical chip select vector to both memory modules [5/28-35]; however, it would have been seen with modified Sandorfi (with the teachings of Haas) that since two 64 MB DRAM memories could have been used [5/28-35] to mirror each other (¶6 of Haas) that the physical chip select vector would have mapped the logical chip select vector to both DIMM modules (as the data in each are mirror, such functionality is thereby inherent).

Allowable Subject Matter

Claims 2,3,8,12, and 13 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action.

Claim 11 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

As per claims 2,8, and 11, the prior art of record does not specifically teach, either alone or in combination all of the limitations of the claims. Specifically, Sandorfi does not teach using a logical chip select vector to index a table and then retrieving the physical chip select from the table; Sandorfi merely teaches converting a logical CS vector to a physical CS vector as shown in figure 3D.

As per claims 3,12, and 13 are allowable as being dependent on allowable base claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Wu et al. (U.S. Patent No. 6,754,797) teaches an address converter that can convert an encoded chip select to a decoded chip select [1/55-63].

Peterson et al. (U.S. Patent Application Publication No. 2003/0128596) teaches in figure 3A multiple DIMM modules 300 being accessed by a chip select vector from memory controller 202.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shane M Thomas whose telephone number is (571) 272-4188. The examiner can normally be reached M-F 8:30 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt M Kim can be reached at (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Shane M. Thomas

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